Amendments to the Specification:

Please add the following paragraph after the paragraph ending on page 3, line 8:

Figure 4 is a block diagram showing two pair of complimentary input/output lines coupled to respective blocks of a bank of memory according to one embodiment of the invention.

Please replace the paragraph starting on line 4 of page 5 with the following amended paragraph:

The operation of the command buffer 74, refresh controller 78 and the SRAM arrays 80, 84 in relation to the other components of the cache system 50 will now be explained with reference to the diagram of Figure 3, which conceptually illustrates the DRAM array 60 and the SRAM arrays 80, 84 shown in Figure 2. As mentioned above, the DRAM array is divided into a plurality of refresh blocks. The refresh blocks may be part of the same or different banks 60a-n of DRAM memory, or physically different DRAM devices. In the embodiment shown in Figure 3, each of the refresh blocks 61a-n has a capacity of Y bits, and each of the SRAM arrays 80, 84 also has a capacity of Y bits. Each of the refresh blocks 61a-n may be individually refreshed under control of the refresh controller 78 (Figure 2). As shown in Figure 4, the DRAM array 60 has twice the normal number of complimentary input/output ("I/O") line pairs 62, which are configured so that two blocks can be simultaneously accessed. More specifically, a first pair 62a of complimentary I/O lines may be coupled to one block 61a of the DRAM array 60 while a second pair 62b of I/O lines may be coupled to another block 61b of the DRAM array 60. As a result, it is possible for data to be read from or written to one refresh block 61a-n of the DRAM array 60 at the same time data are being transferred from one of the SRAM arrays 80, 84 to another block 61a-n of the DRAM array 60.